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LD-2504	Jul.26.'90	A	8 11.7~61.8→10.9~61.0 [Correction]	
	Aug.23.'90	В	6 Table 6 Frequency	2nd Issue
			MIN34→20	
			TYP42→ [Correction]	
	Jan. 10.'91	С	6 Kick-off voltage	3rd Issue
			MIN800-MAX800Vrms [Correction]	
			17&26 Deletion of COCOM Information	
			[Deletion]	
	Ott.08.'91	D	2 Features	4th Issue
			240Vx720H(total 172.800)dots	
			→57,600 pixels [Correction]	
			3 Table 1 Display format	
			57,600 pixels [Correction]	
	Nov. 17. '93	Е	3 Table 1	5th Issue
		<del>-</del>	5.7(diagonal)→14(5.7")cm	
			Outline dimension: MAX-TYP value	
			[Correction]	
			[Note4-1]~ [Addition]	
			, '	
			+115→+ 105, +150→+140,-90→-80,	
			-120110 [Correction]	
			8 : μsec→μs [Correction]	
			9 Table 9 Unit	
			Degree→°(Degree).nt→cd/m²	
			[Correction]	
		ļ	11 2kg-force→19N force, 100g→0.9N	
			[Correction]	
			12 100g→0.9N [Correction]	
			13	
			[Correction]	
			16 Table 10	
			H→h,100G→980m/s² [Correction]	
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#### (1) Introduction

Sharp Color TFT-LCD module is the active matrix LCD (Liquid Crystal Display) produced by making the most of Sharp's expertise in liquid-crystal and semiconductor technologies.

The active device is amorphous silicon TFT (Thin Film Transistor). The module accepts full color video signals conforming to the NTSC(M) and PAL(B·G) system standards.

When additionally provided with the backlight-driving DC/AC inverter and a circuit for producing standard analog R·G·B video signals from composite video signal or micro-computors, it is applicable to pocket TVs and various display monitors.

#### (2) Features

- •Dual mode type (NTSC(M) and PAL(B•G) standards)
- •MBK-PAL, or MaBiKi ("thinning" in Japanese)-PAL which enables the 240-scanning lines panel to display a picture with virtually 280-scanning lines.
- •TFT-active matrix-LCD drive system
- 57,600 pixels (delta configuration)
- •Slim, lightweight and compact
- ① Active-area / 0 utline-area = 5.7 % ② Thickness=23mm ③ Weight=310g
- Built-in video interface circuit and control circuit responsive to two sets of standard R·G·B analog video signals which can be superimpossed.
- High quality full color rendition with backlight source incorporated.
- ·Viewing angle:

```
6 o'clock direction. (LQ6RA01)
12 o'clock direction. (LQ6RA02)
```

#### (3) Construction and Outline

The module consists of a TFT-LCD panel, driver ICs, control PWB mounted with electronic circuits, fluorescent tube, reflector, frame, front and rear shielding cases.

(Backlight-driving DC/AC inverter is not built in the module.)

- \* Illustration of TFT-LCD panel : See Fig. 1.
- \* Construction of TFT-LCD module : See Fig. 2.
- \* Outline dimensions of TFT-LCD module: See Fig. 3.

## (4) Module geometry

Table 1

Parameter	Specifications	Unit	Remarks
Display format	720(W) x240(H)	dots	
Active area	113.8(W) x87.6(H)	mm	ı
Screen size (diagonal)	,14 (5.7")	cm	
Dot pitch	0.158(W) x 0.365(H)	mm	
Dot configuration	R.G.B Delta configuration	- 1	
Outline dimension	149.4(W) x116.4(H) x22.7(D)	mm	[Note 4-1]
Weight	310 ± 20	g	

[Note 4-1] Excluding protrusions.

Dimensions is a TYP value, refer to "Outline dimensions of TFT-LCD module" about details.

## (5) Input / Output terminals

## 5-1) TFT-LCD panel driving section

Table 2

Symbol	∐i/c	Description	Remarks
HSY	0	Internal horizontal sync. signal(In phase with VBS	)
YSY	0	Internal vertical syncsignal(In phase with VBS)	
TST	-	This shall be electrically opened during operational	
N/P	i	Terminal for display mode change of NTSC and PAL	[Note 5-1]
TST	-	This shall be electrically opened during operation	1
ND I	i	Ground	
Vsw	i	Selection signal of two sets of video signals	[Note 5-2]
GND	i	Ground	!
V <sub>свс</sub>	i	DC bias voltage adjusting terminal of common electrode driving signal	[Note 5-3]
VSH	i	Positive power supply voltage	
VBS	i	Composite video signal for sync. separator	[Note 5-4]
BRT i	i   E	Brightness adjusting terminal	[Note 5-5]
VR1 i	C	Color video signal (Red) 1	
VG 1	i	" (Green)1	
VB1	i	(Blue) 1	
VSL	i	Negative power supply voltage	
VR2	i	Color video signal (Red) 2	
VG2	i	(Green)2	
VB2	i	(Blue) 2	
GND	i	Ground	
	HSY   VSY   TST   N/P   TST   N/P   TST   VSW   GND   Vc D C   VSH   VBS   RT   i   VG 1   VSL   VR2   VG2   VB2   VB2	HSY	HSY   0   Internal horizontal sync. signal(In phase with VBS   \overline{VSY}   0   Internal vertical syncsignal(In phase with VBS)     TST   -   This shall be electrically opened during operational   N/P   i   Terminal for display mode change of NTSC and PAL     TST   -   This shall be electrically opened during operation   ND   i   Ground     VSW   i   Selection signal of two sets of video signals     GND   i   Ground     Vcpc   i   Common   electrode   driving signal     VSH   i   Positive power supply voltage     VSB   i   Composite video signal for sync. separator     BRT   i   Brightness adjusting terminal     VR1   i   Color video signal (Red)   1     VSI   i   Negative power supply voltage     VR2   i   Color video signal (Red)   2     VG2   i   (Green)   2     VG2   i   (Green)   2     VB2   i   (Blue)   2     VB3   i   (Blue)   2     VB4   i   (Color video signal (Red)   2     VG2   i   (Green)   2     VG2   i   (Green)   2     VG3   i   (Green)   2     VG4   i   (Green)   2     VG5   i   (Green)   2     VG6   i   (Green)   2     VG7   i   (Green)   2     VG8   i   (Green)   2     VG9   i   (Green)   2

In the following descriptions, "High" means "Vs " and "Low" means "GND".

[Note 5-1] Selects display mode.

- ① When  $N/\bar{P}$  is "High" or open, the module operates in NTSC(M) mode.
- ② When  $N/\overline{P}$  is "Low", the module operates in PAL(B•G) mode.
- [Note 5-2] Selects a set of  $R \cdot G \cdot B$  video signals.
  - ① When VSW is "High" of open, video signal set 1 (Pin NOS 13 through 15) is selected.
  - When VSW is "Low", video signal set 2(Pin NOS 17 through 19) is selected.
- [Note 5-3] Common electrode driving  $signal(V_{com})$  generated in the module is observed on the pin. Should be opened during operation, as the DC component of  $V_{com}(V_{com})$  is adjusted to the optimum value with  $V_{sh}$  and  $V_{sh}$  being the typical values on shipping.

But, in case of change of the optimum value (for example, lowering of the power source), it should be re-adjusted by the built-in variable resistor  $(V_{\text{CDC}})$  or external circuit shown in Fig. 5.

Refer to (Appendix-3) "Adjusting method of optimum common electrode DC bias voltage" for re-adjusting.

- [Note 5-4] Responsive to standard composite sync. signal with negative polarity of the same amplitude level as that of the composite video signal.
- [Note 5-5] Brightness (black level of video signal) is adjusted by the DC voltage supplied to the pin.

Brightness is adjusted to the optimum value on shipping, but, it can be re-adjusted by the built-in variable resistor (BRT) or external circuit shown in Fig. 5.

#### 5-2) Backlight driving section

Table 3

PinNo.	Symbol	i/o	Description	Remarks
L1	VL 1	i	Power supply for fluorescent tube 1(GND)	[Note 5-6]
L2	NC	-	No connection	
L3	VL 2	i	Power supply for fluorescent tube 1(High voltage)	
L4	VL 3	i	Power supply for fluorescent tube 2(High voltage)	
L5	NC	-	No connection	
L6	VL 4	0	Power supply for fluorescent tube 2(GND)	[Note 5-6]

[Note5-6] Should be grounded by the backlight driving DC/AC inverter, as the L1 and L6 terminals are connected with the shielding film in the module .

These terminals will be grounded by the optional DC/AC inverter. (For internal electrical connection of backlight unit, see Fig.(i) below.)

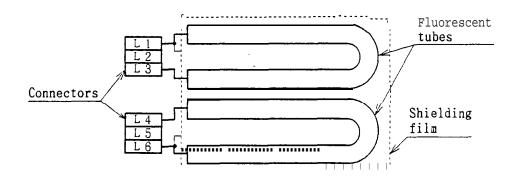


Fig.(i) Wiring diagram of backlight unit

#### (6) Absolute maximum ratings

Table 4 GND=0V Ta=25r

Parameter	Symbol	MIN	MAX	Unit	Remarks	
Positive power supply	voltage	V <sub>s H</sub>	-0.3	+6.0	V	
Negative power supply	voltage	V S L	-9.0	+0.3	V	
Analog input signals		Vi	_	2.0,	Vр −р	[Note 6-1]
Digital input/output s	ignals	VI	-0.3	V <sub>sн</sub> +0.3	V	[Note 6-2]
DC bias voltage of common electrode driv	ingsignal	V <sub>CDC</sub>	V <sub>s L</sub> -0.3	-1.5	V	
Brightness adjusting t	erminal voltage	V <sub>BRT</sub>	-0,3	V <sub>s H</sub> +0.3	V	
Storage temperature	Tstg	-25	60	r		
Operating temperature	Topp	0	60	T.	[Note 6-3]	
	Ambient temp.	Topa	0	40	٢	

[Note 6-1] VBS, VR1, VG1, VB1, VR2, VG2, VB2 terminals (Video signal)

[Note 6-2]  $\overline{\text{HSY}}, \overline{\text{VSY}}, \text{VSW}, \text{N/$\overline{P}$}$  terminals

[Note 6-3] Maximum wet-bulb temperature  $38\ensuremath{\mathtt{T}}$  or less. No dew condensation.

- (7) Electrical characteristics
- 7-1) Recommended operating conditions
- A) TFT-LCD panel section

Table 5

GND=0V Ta=25°C

Paramet	er	Symbol	MIN	TYP	MAX	Unit	Remarks
Positive power	supply voltage	V <sub>s H</sub>	+4.8	+5.0	+5.2	V	
Negative power	supply voltage	V <sub>s</sub> L	-7.6	-8.0	-8.4	V	
Analogue input	Amplitude	VBS	0. 7	1. 0	1. 3	Vp-p	[Note7-1]
voltage		Vi	_	0.7	_	Vp-p	[Note7-1,2]
	DC component	Vipc	-1.0	0	+1.0	V	[Note7-3]
Digital input	High level	v,H-	+3.5	_	VsH	V	[Note7-4]
voltage	Low level	VIL	0	_	+1.5	V	
Digital output	High level	V <sub>OH</sub>	+3.5	_	V <sub>s H</sub>	V	[Note7-5]
voltage	Low level	Vor	0	-	+1.5	V	
DC bias voltage electrode driv	V <sub>c D c</sub>	-4.5	-3.5	-2.5	V	[Note7-6]	
Terminal volta brightness adju	stment	V <sub>BRT</sub>	1. 2	2. 2	3. 2	V	

[Note/-1] input Impedance : >20k!

[Note7-2] VR1, VG1, VB1, VR2, VG2, VB2 terminals (Video signals)

[Note7-3] VBS, VR1, VG1, VB1, VR2, VG2, VB2 terminals (Video signals)

[Note7-4]  $N/\bar{P}$ , VSW terminals

Input impedance :  $>50k\Omega$ 

[Note7-5] HSY, VSY terminals (Internal sync. signals) .

Load resistance :  $>20k\Omega$ 

[Note7-6] Adjusted for each module so as to attain maximum contrast ratio.

Refer to (Appendix-3) for adjusting.

#### B) Backlight driving section

Table 6

Ta=25°C

Parameter	Symbol	MIN	TYP	MAX	Unit	Remarks
Lamp voltage	VL	290	330	370	Vrms	(just for reference)
Lamp current	IL	6.0	7.0	8.0	mArms	
Frequency	f′	20		50	kHz	
Kick-off voltage	٧s	_	_	800	Vrms	

 $\times$  DC/AC inverter for driving cold cathode fluorescent tube (CCFT) is not built in the module.

DC/AC inverter for external connection (Model No.: LQ0J04) is optionally available.

#### 7-2) Power' consumption

Table 7

Ta=25℃

Para	Symbol	Condition	HIN	TYP	MAX	Unit	Remarks	
Power	Positive supply current	Isu	$V_{SH} = +5.0V$	-	+105	+140	πA	
consumption by the pane	Negative  supply_current	IsL	$V_{sL} = -8.0V$	_	-80	-110	mΑ	
section	Total	Ws	0.5	_	1.30	1.71	W	[Note7-7]
	Power consumption by the fluorescert tube section			-	4.6	6.0	W	[Note7-8]

[Note7-7] Excluding power consumption by the backlight.

[Note7-8] Calculated reference value ( $I_L \times V_L$ ).

### 7-3) Circuit diagram

The circuit block diagram of TFT-LCD module is shown in Fig.4.

(For detail, refer to (Appendix-1) and (Appendix-2).

The recommended external circuit for TFT-LCD module is shown in Fig.5.

Caution: Turn on or off the power supply (V<sub>SH</sub> and V<sub>SL</sub>) at the same time.

Be sure to supply all power voltages before inputting input signals.

## 7-4) Input/Output signal waveforms

Shown in Fig. 6

Caution: For the VBS signal, input standard composite video (or sync.) signal applicable to the operating mode selected by the  $N/\overline{P}$  signal.

A long time input of non-standard sync. signal may cause flicker or degradation of display quality.

#### 7-5) Input/Output signal timing chart

Shown in Fig. 7.

Table 8 shows the timing specifications.

Table 8

NTSC(M):f,,=15. 7kHz.fv=60Hz PAL(B, G):f,,=15. 6kHz,fv=50Hz

Para	Symbol	MIN	TYP	MAX	Uni	ti Remarks	
Horizontal	Input pulse width	T H S I	4.2	4.7	5.7	μs	
sync.	Output pulse width	τ н s 2	2.3	3.0	4.6	μs	f=f" [Note7-9]
Horizontal	sync.phase difference	τpd	-1.5		1.3	μs	[Note7-10]
Vertical sy	τVs	243	256	269	μѕ	4/f <sub>H</sub>	
Vertical sy	r pv	67/33	73/39	79/45	μѕ	[Note7-11]	

(Supply voltage condition:  $V_{SH}=+5V, V_{SL}=-8V$ )

[Note7-9] Adjusted by variable resistor (H-POS).

[Note7-10] Variable range by variable resistor (H-POS)
(Positive when HSY proceeds VBS.)

Adjusted value :  $\tau pd = -0.1 \pm 0.7 \mu s$ 

[Note7-11] Odd field/Even field  $(1/f_H/0.5/f_H)$ 

### 7-6) Display time range

- ① When sync. signal of NTSC(M) system is applied.
  - (a) Horizontally

11 .7-61.8 µs from the falling edge of HSY.

(b) Vertically

19~258H from the falling edge of VSY.

- ② When sync. signal of PAL(B.G) system is applied.
  - (a) Horizontally

11 .7-61.8  $\mu$ s from the falling edge of  $\overline{\text{HSY}}$ .

(b) Vertically

 $25 \sim 304 \text{H}$  from the falling edge of VSY.

The video signals of (14n+12)H.(14n+20)H/Even field, (14n+17)H.(14n+23)H/Odd field  $(n=1,2,3,\ldots,20)$  are not displayed on the module.

## (8) Optical characteristics

Table 9  $Ta=25^{\circ}$ 

Parameter /.			. Symbol Condition MIN		TYP	MAX	Unit	Remarks
Viewing angle range		1911	CR≧10	30(10)	_	_	0	LQ6RA01
		Δθ 12	CR210	10(30)	_	_	(Degree)	(LQ6RA02)
		Δθ2	CR≧10	45	_	_		[Note 8-1,2]
Contrast ratio		CRmax	Optimum	60	_	_		[Note 8-2,3]
Response	Rise	τr	viewing	_	30	60	ms	[Note 8-2]
time	Decay	r d	angle	-	50	100	ms	[Note 8-4]
Brightness		Yı		100	120	_	cd/m²	
Color temperature		Kι	$\theta = 0^{\circ}$ .	_	7900	_	K	[Note 8-5]
White chromaticit		у ж	•	0.247	0.297	0.347		
		ÿ		0.262	0.312	0.362		

[Note 8-1] Viewing angle range is defined as follows.

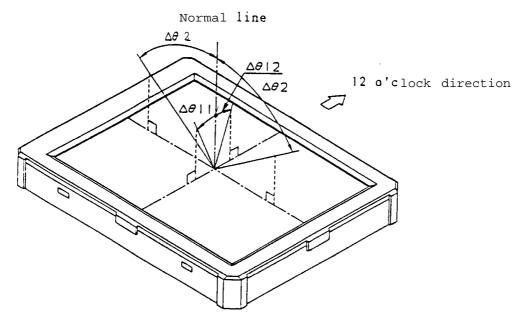


Fig. (ii) Definition of viewing angle range

[Note 8-2] Applied voltage for measuring optical characteristics

- a)  $V_{cpc}$  must be adjusted by the (1) Flicker measuring method or the (2) Contrast measuring method described in the (Appendix-3) "Adjusting method of optimum common electrode DC bias voltage."
- b) Brightness adjusting terminal (BRT) should be opened.
- c) Video signal of reference black level and 100% white level must be input.

[Note 8-3] Contrast ratio is defined as follows.

Contrast ratio is calculated with the following formula in the optical characteristics measuring method shown in Fig. 8.

Contrast ratio (CR)

# = Photodetector output with LCD being "white" Photodetector output with LCD being "black"

[Note 8-4] Input signals are applied to the area measured to make the area "white" and "black" respectively, and change with time in the photodetector output is measured in the optical characteristics measuring method shown in Fig. 8.

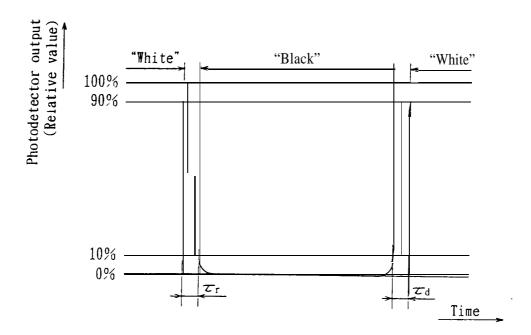


Fig. (iii)

[Note 8-5] Measured on the center area of the panel at a viewing cone 1° by TOPCON luminance meter BM-7. (After 10 minutes operation)

#### (9) Mechanical characteristics

#### 9-1) External appearance

There shall not be any conspicuous defects. (See Fig. 3. "Outline dimensions of TFT-LCD module".)

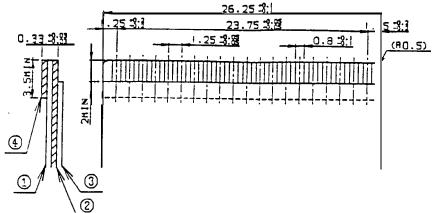
### 9-2) Panel toughness

The panel shall not break when the panel center is pressed with 19N force by 15 mm dia. smooth flat surface.

(Caution): The least force can cause functional troubles if it is applied on the active area for a long time.

#### 9-3) 1/0 connector performance

- A) 1/0 connector of LCD panel driving circuit (FPC connector 20 pins)
  - i) Applicable FPC: Shown in Fig. (iv).
  - U) Terminal holding force: 0.9N or larger/pin(Each terminal is pulled out at a rate of 25 ± 3 mm/min.)
  - ii) Insertion/pulling durability: Contact resistance not larger than double the initial value after applicable FPC is inserted and pulled out 20 times.



Ref. No	Name	Material	
1	Base material	Polyimide or equivalent material (25 mm thick)	
2	Copper foil	Copper foil (352m thick). solder plated in <b>2</b> to 122m thickness	
3	Coverlay	Polyimideor equivalent material	
4	Reinforcing plate (1882 the thick)		

Fig. (iv) Applicable FPC for 1/0 connector (1.25 mm pitch)

- B) 1/0 connector of backlight driving circuit (XH connector 3 pins x2 PCs.)
  - i) Applicable connector housing: XHP-3 (produced by Japan Solderless Terminal)
  - i) Terminal holding force: 0.9N or more/pin (Pulled out at a rate of 1 through 5 mm/s .)
  - in) Insertion/pulling durability: Contact resistance not larger than double the. initial value after connectors are inserted and pulled out 20 times.

## (10) Display quality

The display quality of the color TFT-LCD module shall be in compliance with the Delivery Inspection Standard (Separate Sheet LDI-90522).

## (11) Handling instructions

#### 11-1) Mounting of module

The TFT-LCD module is designed to be mounted on equipment using the mounting tabs in the four corners of the module rear face.

On mounting the module, as the M3 tapping screw (fastening torque is 0.5 through 0.6 N·m) is recommended, be sure to fix the module on the same plane, taking care not to warp or twist the module.

#### 11-2) Precautions in mounting

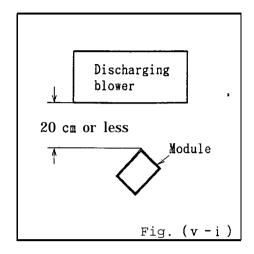
- ① Polarizer which is made of soft material and susceptible to flaw must be handled carefully. Protective film (laminator) is applied on the surface to protect it against scratches and dirts. It is recommended to peel off the laminator immediately before the use, taking care of static electricity.
- 2 Precautions in peeling off the laminator
  - A) Working environment

When the laminator is peeled off. static electricity may cause dust to stick to the polarizer surface. To avoid this, the following working environment is desirable.

- a) Floor: Conductive treatment of 1  $M\Omega$  or more on the tile (Conductive mat or conductive paint on the tile)
- b) Clean room free from dust and with an adhensive mat on the doorway
- c) Humidity: 50 % to 70 % RH
- d) Workers shall wear conductive shoes. conductive work. clothes. conductive gloves and an earth band.

#### B) Working procedures

- a) Direct the wind of discharging blower somewhat downward to ensure that module is blown sufficiently, Keep the distance between module and discharging 'blower within 20 cm. (See Fig. (v-i).)
- b) Attach adhensive tape to the laminator part near discharging blower so as to protect polarizer against flaw. (See Fig. (v -ii).)
- c) Peel off laminator. pulling adhensive tape slowly to your side taking 5 or more second.
- d) On peeling off the laminator, pass the module to the next work process to prevent the module to get dust.



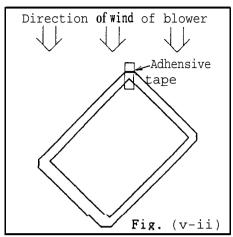


Fig. (v)

- e) Method of removing dust from polarizer
  - $^{\circ}$  Blow off dust with N<sub>2</sub> blower for which static electricity preventive measure has been taken. Ionized air gun (Hugle Electronics Co.) is recommended.
  - Since polarizer is vulnerable, wiping should be avoided. If wiping is unavoidable, wipe it carefully with lens cleaning cloth, breathing on it. "Belleseime" (Kanebo, Ltd.) is desirable.
- When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth. For stubborn dirts, wipe the part, breathing on it.
- ④ Wipe off water drop or finger grease immediately. Long contact with water may cause discoloration or spots.
- (5) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Handle with care.
- 6 Since CMOS LSI is used in this module, take care of static electricity and earth your body when handling.

#### 1 1-3) Precautions in adjusting module

Adjusting volumes on the rear face of the module have been set optimally before shipment. Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described here may not be satisfied.

#### 11-4) Others

- ① Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours; liquid crystal is deteriorated by ultraviolet rays.
- ② Store the module at a temperature near the room temperature. At lower than the rated storage temperature, liquid crystal solidifies, causing the panel to be damaged. At higher than the rated storage temperature, liquid crystal turns into isotropic liquid and may not recover.
- ③ If LCD panel breaks, there may be a possibility that the liquid crystal escapes from the panel. Since the liquid crystal is injurious, do not put it into the eyes or mouth. When liquid crystal sticks to hands, feet or clothes, wash it out immediately with soap.
- ① Observe all other precautionary requirements in handling general electronic components.

#### (12) Shipping requirements

12-1) Packing form is shown in Fig. 9.

#### 12-2) Carton storage condition

- ① Number of layers of cartons in pile : 10 layers Max.
- ② Environmental condition :

• Temperature 0 to 40 t

 $^{\circ}$  Humidity 60 %RH or less (at 40 %)

No dew condition even at a low temperature and

high humidity

Atmosphere Harmful gases such as acid and alkali which corrode

electronic components and wires must not be

detected.

" Storage period About 3 months

Opening of package To prevent TFT-LCD module from being damaged by

static electricity, adjust the room humidity to

50 %RH or higher and provide an appropriate measure for electrostatic earthing before opening the

package.

#### (13) Reliability test items

Reliability test items for the TFT-LCD module are shown in Table 10.

## Reliability Test Items for TFT-LCD Module

Table 10

No. Test items		Conditions
1	High temperature	T a = 60°C 240 h
	storage test	•
2	Low temperature	$T a = -25 ^{\circ}C$ 2 4 0 h
	storage test	
	High temperature	
3	and high humidity	$T a = 40 \text{ °C} \cdot 95 \text{ % R H}$ 2 4 0 h
	operation test	
4	High temperature	$T a = 40 ^{\circ}C$ 2 4 0 h
	operation test	
5	Low temperature	T a = 0 c 2 4 0 h
	operation test	
6	Electrostatic	$\pm 200 \text{ V} \cdot 200 \text{ pF} (0\Omega)$ Once for each terminal
	discharge test	
7	Shock test	9 8 0 m/s <sup>2</sup> · 6 ms, $\pm X$ ; $\pm Y$ ; $\pm Z$ 3 times for each direction
		(JIS C7021, A-7 Condition C)
		Frequency range: 1 0-5 5 Hz
		Stroke : 1.5 mm
8	Vibration test Sweep : 1 0 Hz ~ 5 5 Hz ~ 1 0 Hz	
		2 hours for each direction of X,Y,Z (6 hours in total
		(JIS C7021, A-10 Condition A)
9	Heat shock test	$-25^{\circ}\text{C} \sim +60^{\circ}\text{C} / 5 \text{ cycles}$ (2 hours/cycle)
		(1b) (1b)

## [ Result Evaluation Criteria ]

Under the display quality test conditions with normal operation state, there shall be no change which may affect practical display function.

#### (14) Others

If any problem occurs in relation to the description in the present specifications or other relevant items, it shall be eliminated in all sincerity through discussion.

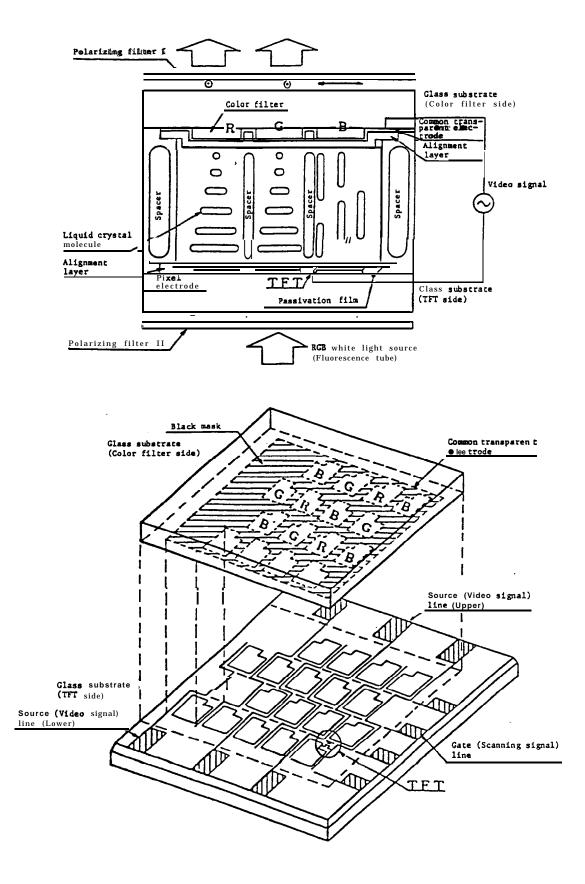


Fig. 1 Illustration of TFT-LCD panel

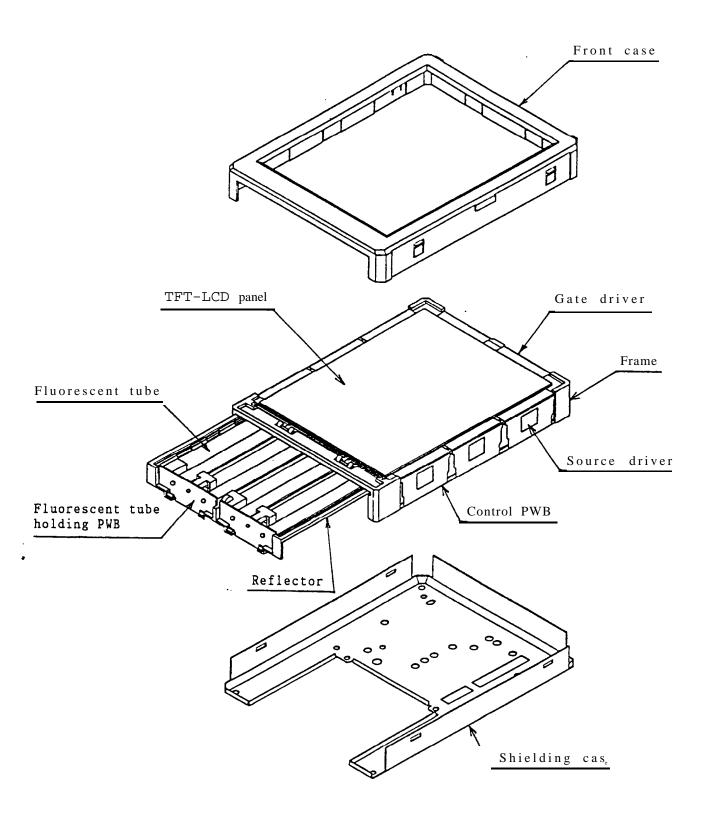
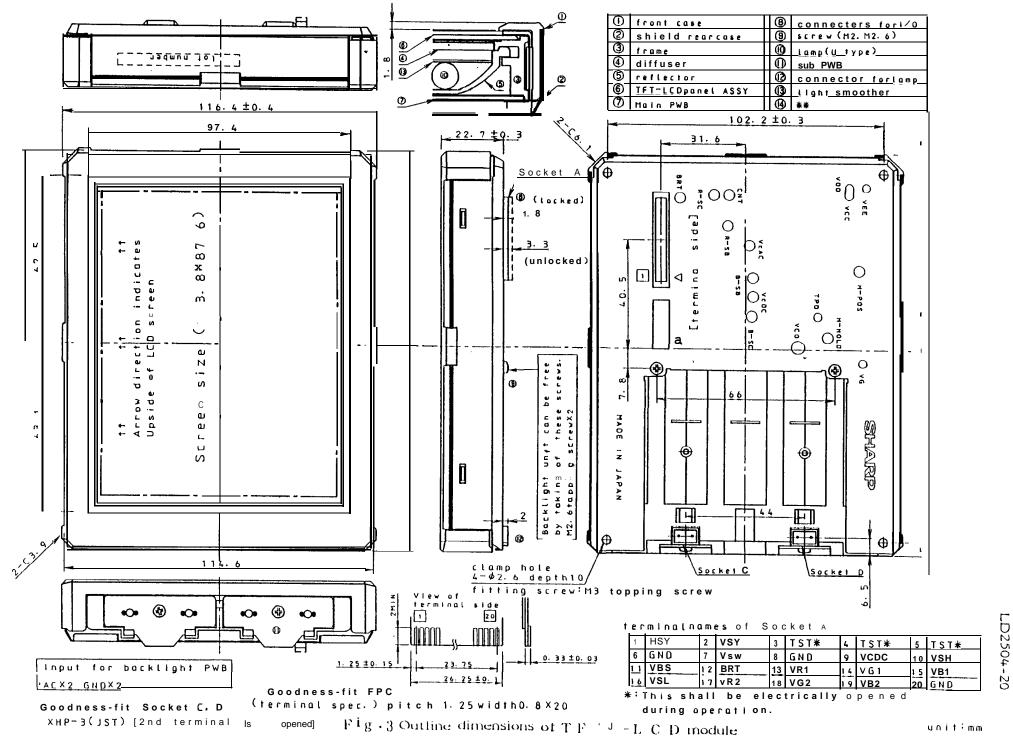


Fig. 2 Construction of TFT-LCD module



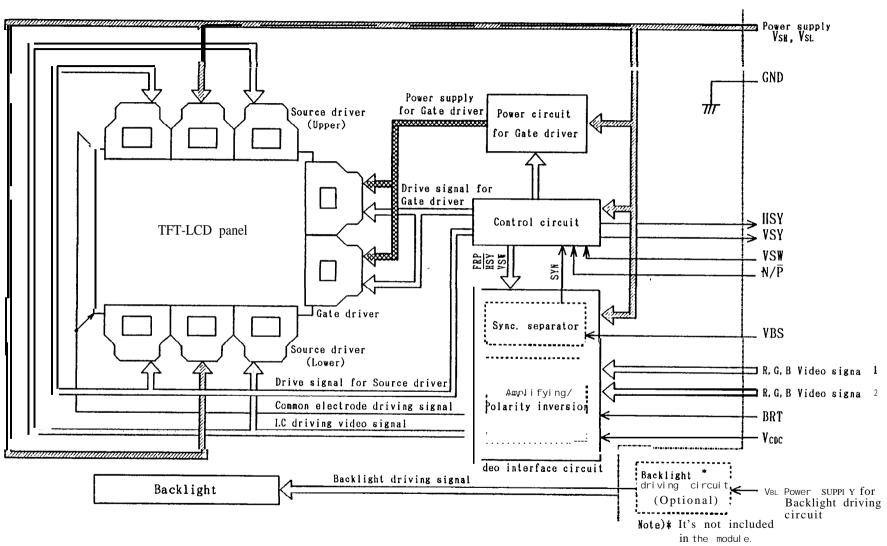


Fig. 4 Circuit block diagram of TFT-LCD module

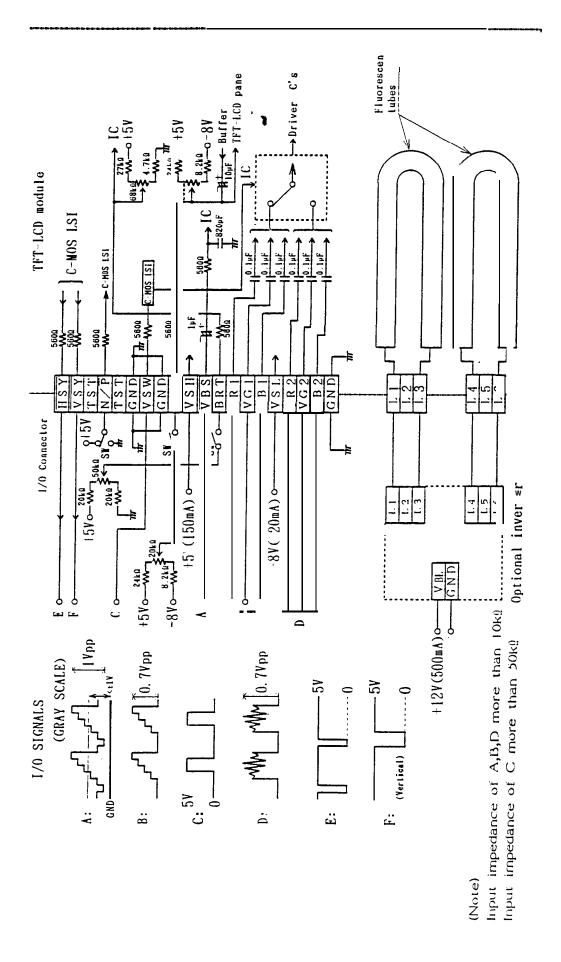


Fig. 5 Recommended circuit for TFT-LCD module

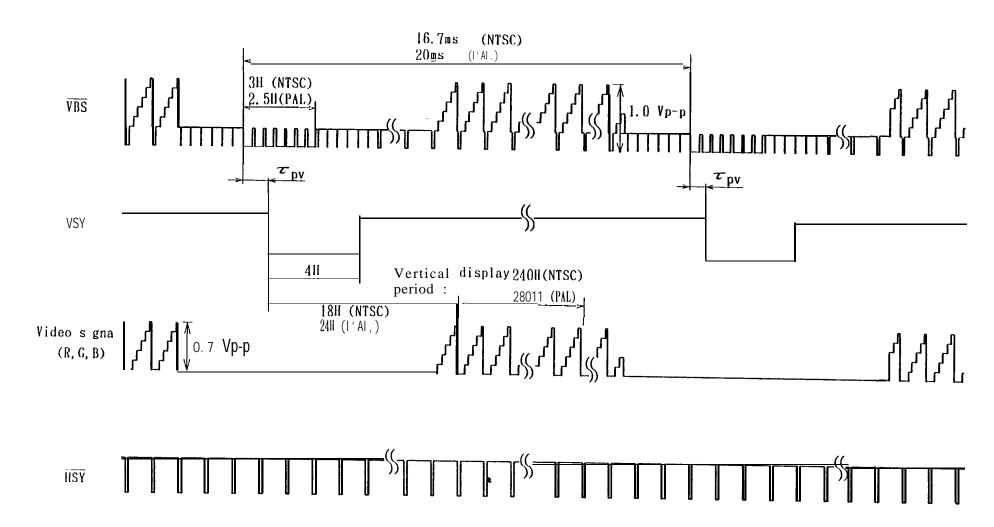


Fig. 6 Input/Output signal waveforms

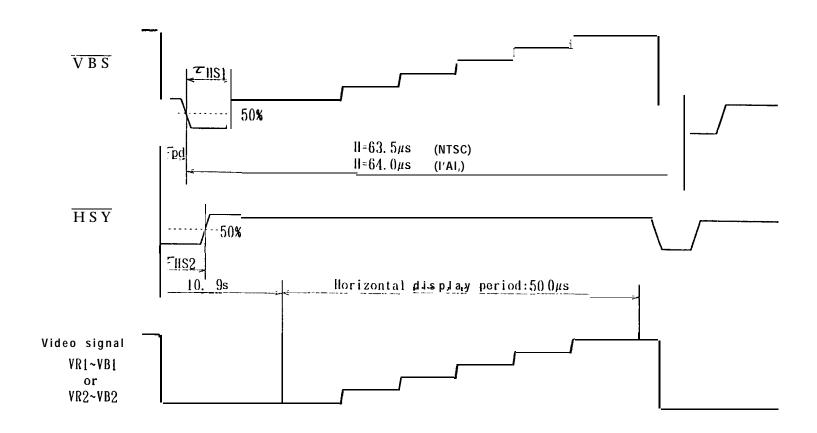


Fig. 7Input/Output signal timing chart

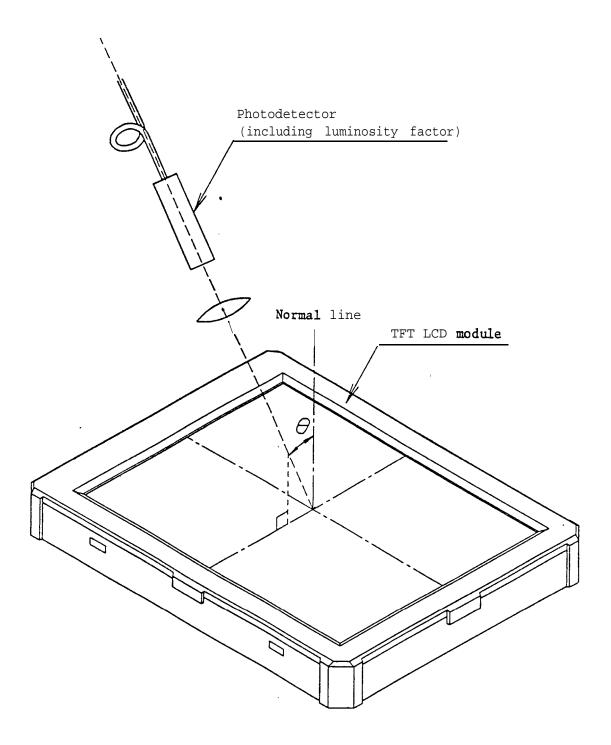


Fig. 8 Optical characteristics measuring method

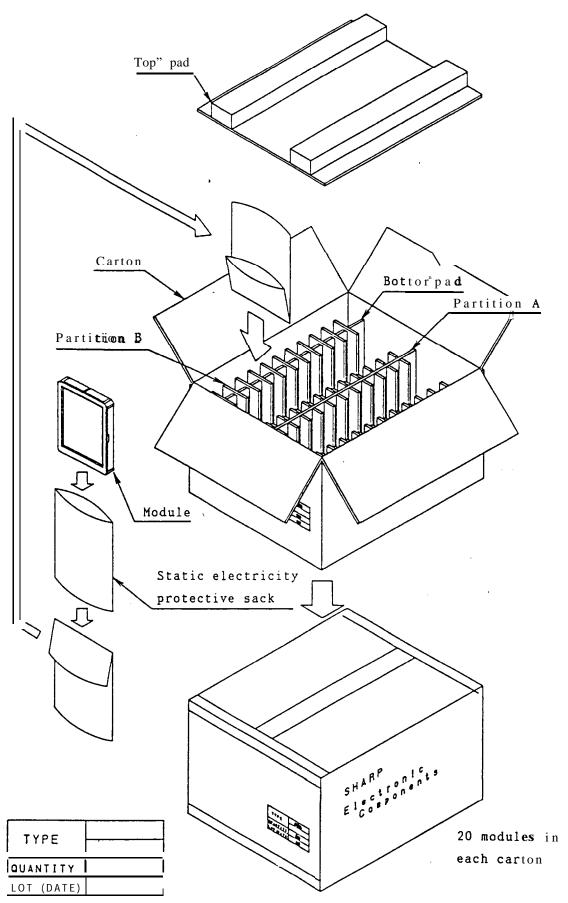


Fig. 9 Packing form

#### (Appendix-1)

#### ≪ Construction of TFT-LCD module »

TFT-LCD module is composed of an LCD panel, driver ICS for the LCD panel, a control circuit for the driver ICs, a video signal processing circuit (video interface circuit) peculiar to LCD, and a backlight.

The driver ICs are divided into two types: a source driver (data driver) which receives R•G•B signals and sends them sequentially by one horizontal line of the LCD panel, and a gate driver (scan driver) which scans 240 gate lines of the LCD panel,

The circuit diagram is shown in Fig.4.

for both of the inputs to the module.

The module displays an image on LCD panel as it receives power supplies  $(V_{SH},V_{SL})$ ,  $R \cdot G \cdot B$  video signals, DC bias voltage of common electrode driving signal  $(V_{CDC})$ , composite video signal or composite synchronizing signal  $(\overline{VBS})$ , selection signal of two sets of video signals (VSW) and brightness adjusting DC voltage (BRT) from the exterior.

The composite video signal is subject to synchronous separation in the module and used to write a video signal accurately on each pixel on the module,

The control circuit receives composite synchronizing signal separated in the video interface circuit, generates clock pulses synchronized with the composite synchronizing signal and gate and source drivers-driving signals, and outputs internal horizontal synchronizing signal ( $\overline{\text{HSY}}$ ), internal vertical synchronizing signal ( $\overline{\text{VSY}}$ ) and polarity inversion signal (FRP).

The voltage level of R·G·B video signals applied to the liquid crystal layer of each pixel through the source driver IC and TFT is about 3.7 Vp-p from black to white level. In order to prevent the electro-chemical decomposition of the liquid crystal, it is necessary to apply AC voltage to the liquid crystal, For this purpose, the polarity of the video signals must be alternated. Since the amplification and polarity inversion of the video signals are performed in the video interface circuit in the module using the polarity inversion signal (FRP), standard analog R·G·B signals of 0.7 Vp-p may be used

Power supplies to this module are ① 5 V ( $V_{SH}$ ),② O V (GND), and ③ -8 V ( $V_{L}$ ). Control IC operates on O to 5 V line so that it outputs HSY and VSY at 0 to 5 V level. Power supplies to the video interface circuit are  $V_{SH}$  and  $V_{SL}$ .

VSW is used to select either of two sets of  $R \cdot G \cdot B$  video signals.

VSW selects the first set of video signals when it is "High" or open, and selects the second set when it is "Low".

 $N/\bar{P}$  is used to select display mode.

When it is "High" or open, the module operates in NTSC(M) mode, and when it is "Low", the module operates in  $PAL(B \cdot G)$  mode.

BRT and  $V_{c\,D\,c}$  are adjusted to the optimum value on shipping.

The module contains backlight (cold cathode fluorescent tubes) butnota driving circuit for the backlight. Therefore, it is necessary to install a DC/AC inverter for driving the fluorescent tubes.

Standard DC/AC inverter (Model name: LQ0J04) is available as an option.

In addition, the backlight of the module is designed to be replaceable,— and backlight unit (Model name: LQOBO4) is available as a service part for the replacement.

(Appendix-2)

#### **《** Example of TFT-LCD TV ≫

Fig.A shows a block diagram example of the TFT-LCD module applied to a TV set.

The block enclosed by is the TFT-LCD module.

Other signal processing systems are the same as those in ordinary CRT-TVs.

The following six signals must be supplied to this module from the exterior:

- ① Composite video signal: VBS
- ② Standard analog R·G·B video signals in two sets
- $\mathfrak{J}$  Signal for changing display mode:  $\mathbb{N}/\overline{\mathbb{P}}$
- Signal for selecting input video signals: VSW
- $\mathfrak{S}$  DC bias voltage of common electrode driving signal:  $V_{\text{cpc}}$
- 6 Brightness adjusting DC voltage: BRT

The following two signals are output from this module to the exterior.

- ① Internal horizontal synchronizing signal: HSY
- 2 Internal vertical synchronizing signal: VSY

When this module is applied to a TV set, for example, HSY and  $\overline{\text{VSY}}$  are used to display selected channel number and characters an the screen.

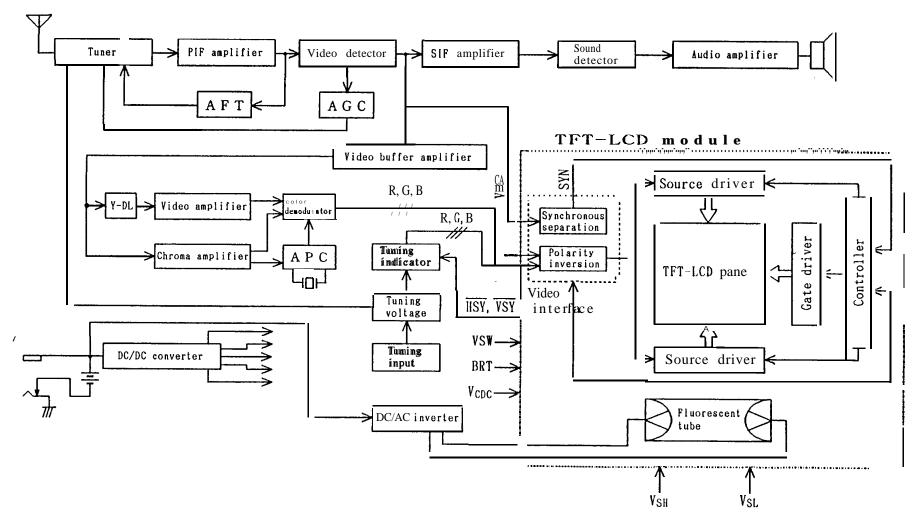


Fig. A Block diagram of TFT-LCD TV set

(Appendix-3)

#### Adjusting method of optimum common electrode ${\tt DC}$ bias voltage

To obtain optimum DC bias voltage of common electrode driving  $signal(V_{cDC})$ , photo-electric devices are very effective, and the accuracy is within 0.1V.

(In visual examination method, the accuracy is about 0.5V because of the difference among individuals.)

To gain optimum common electrode DC bias voltage, there are two methods which use photo-electric devices. The value of optimum DC bias voltage is the same in both methods.

#### () Measurement of flicker

DC bias voltage is adjusted so as to minimize NTSC:60Hz(30Hz) flicker. PAL:50Hz(25Hz)

#### (2) Measurement of contrast

DC bias voltage is adjusted so as to minimize the **photo-electric** output voltage.

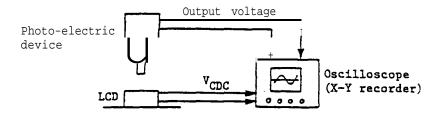


Fig. B Measurement system

#### (1) Measurement of flicker

Photo-electric output voltage is measured by an oscilloscope at a system shown in Fig.B.

DC bias voltage must be adjusted so as to minimize the NTSC: 60Hz(30Hz) flicker with DC bias voltage changing slowly. (Fig,C)

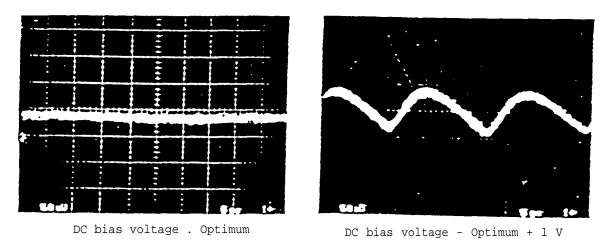


Fig.C Waveforms of flicker

#### (2) Measurement of contrast

Photo-electric output voltage is measured by oscilloscope or X-Y recorder by using the system in Fig.A. Common electrode DC bias voltage must be adjusted so as to minimize the photo-electric output voltage with DC bias voltage changing slowly. (Fig.D)

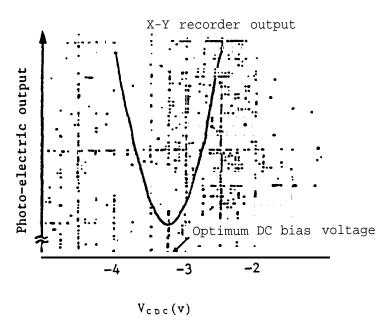


Fig.D Optimum common electrode DC bias voltage by measurement of contrast

#### (3) Notes

① Measurement is more accurate at half tone as compared with other gradation level.

(Change of photo-electric output is small at black level.) see Fig. E.

② DC bias voltage must be adjusted slowly. The value of optimum common electrode DC bias voltage changing fast is different from that with changing slowly.

Because DC response is slow. see Fig.F.

The final adjustment of DC bias voltage must be made by changing from positive to negative.

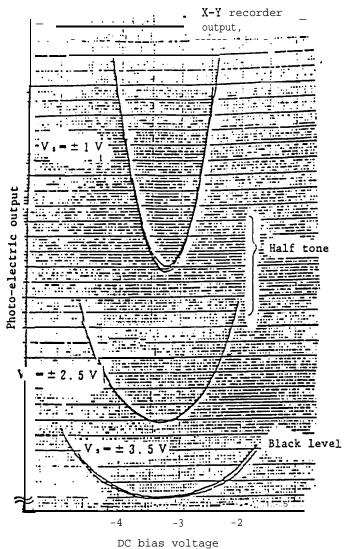


Fig.E Relation between gradation

level and DC bias voltage

Optimum common electrode DC bias voltage is almost equal between half tone and black level.

But it is difficult to deside the optimum point at black level.

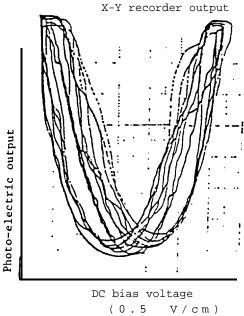


Fig.F Output voltage with DC bias

voltage changing fast

The value of minimum point is not definite because DC response is slow.

And optimum point cannot be attained,